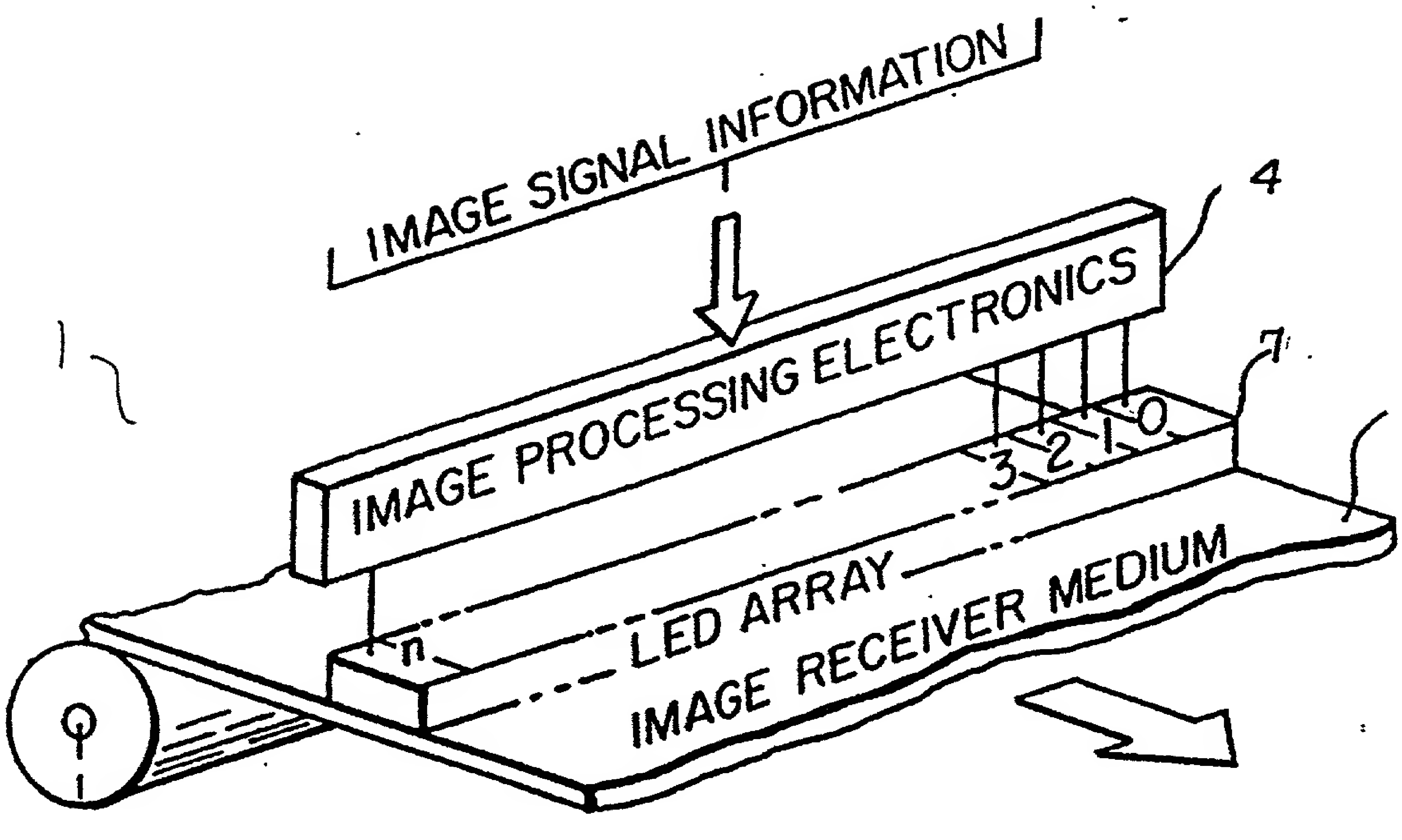


FIG. 1
PRIOR ART

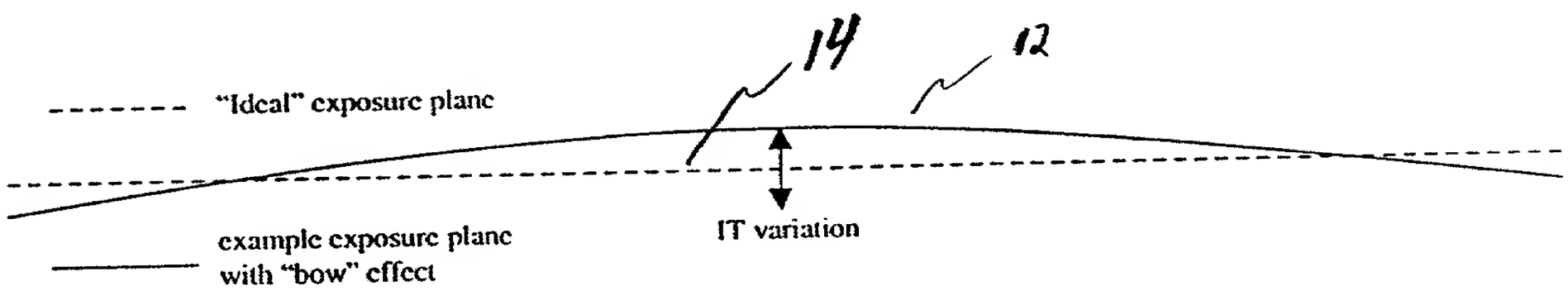


Figure 2a

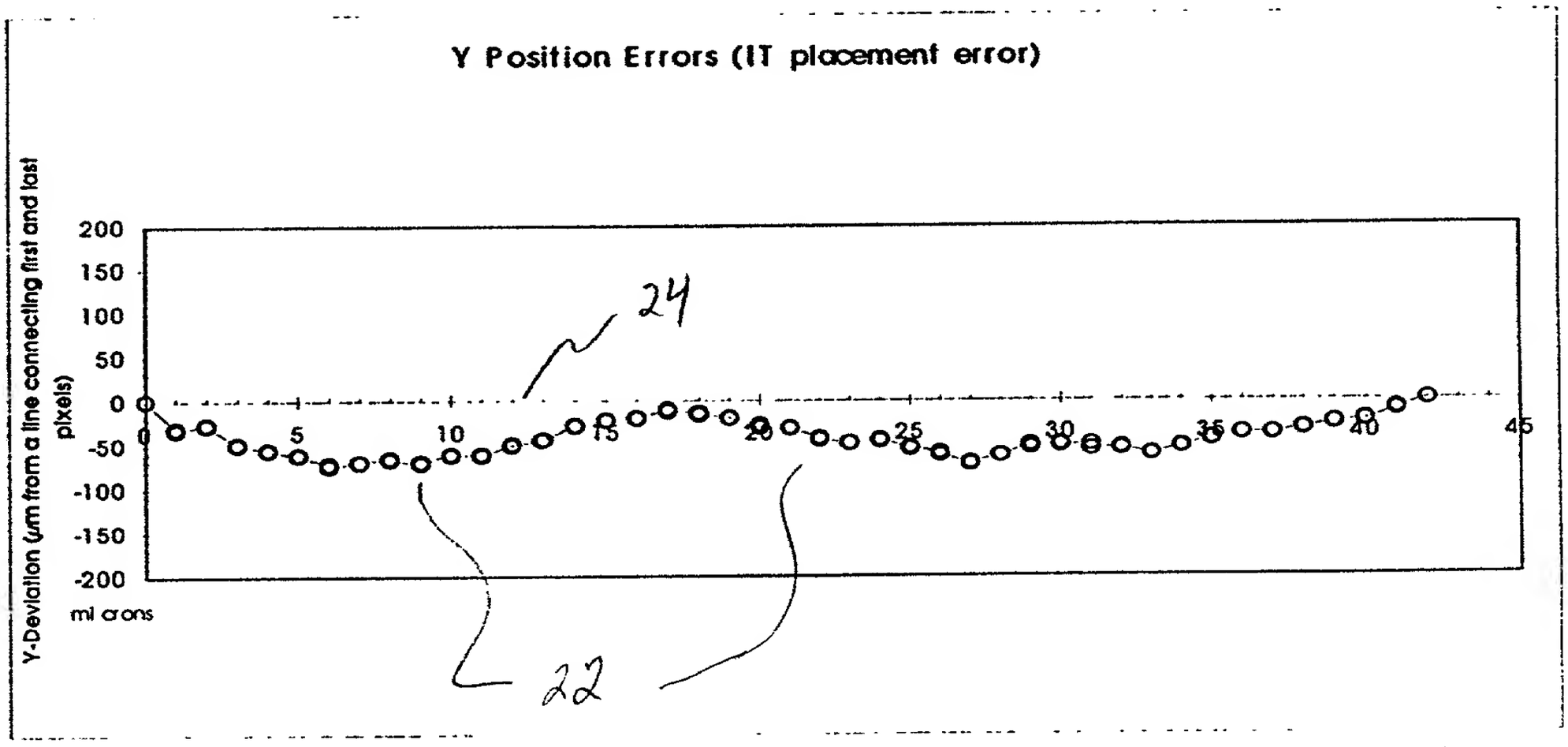


Figure 2b

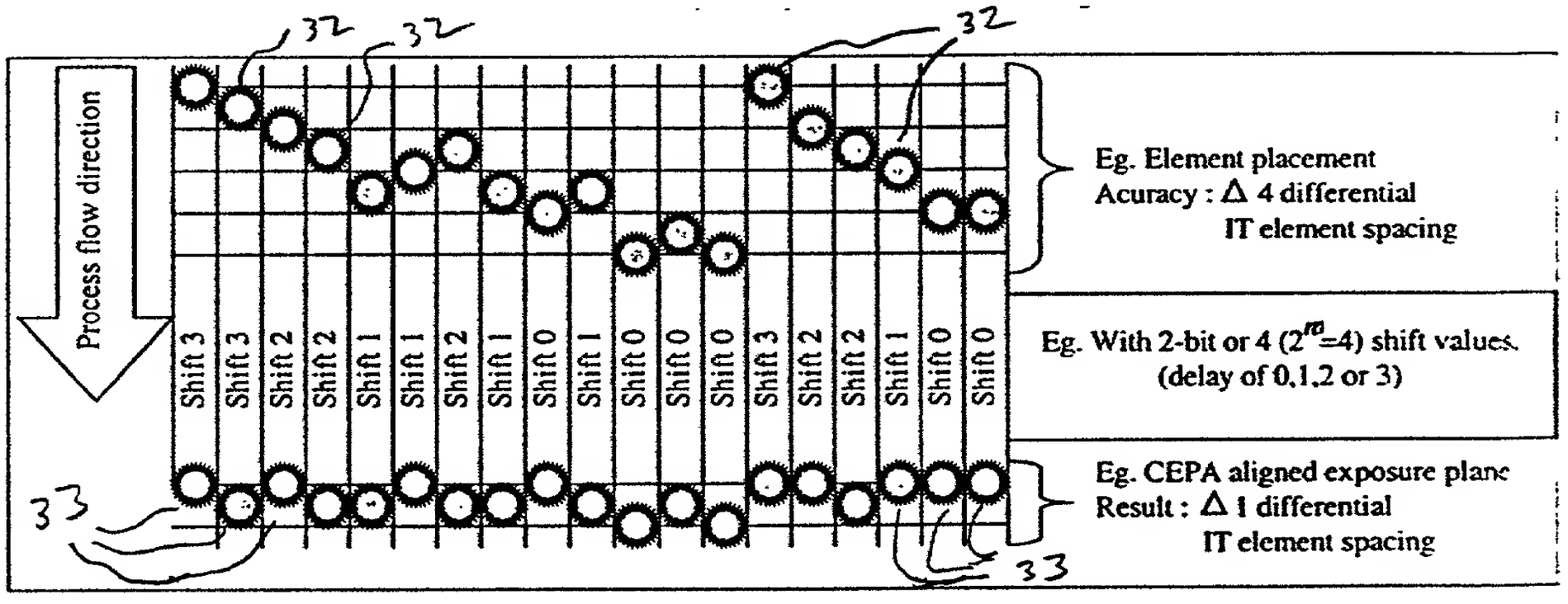


Figure 3 CEPA alignment example

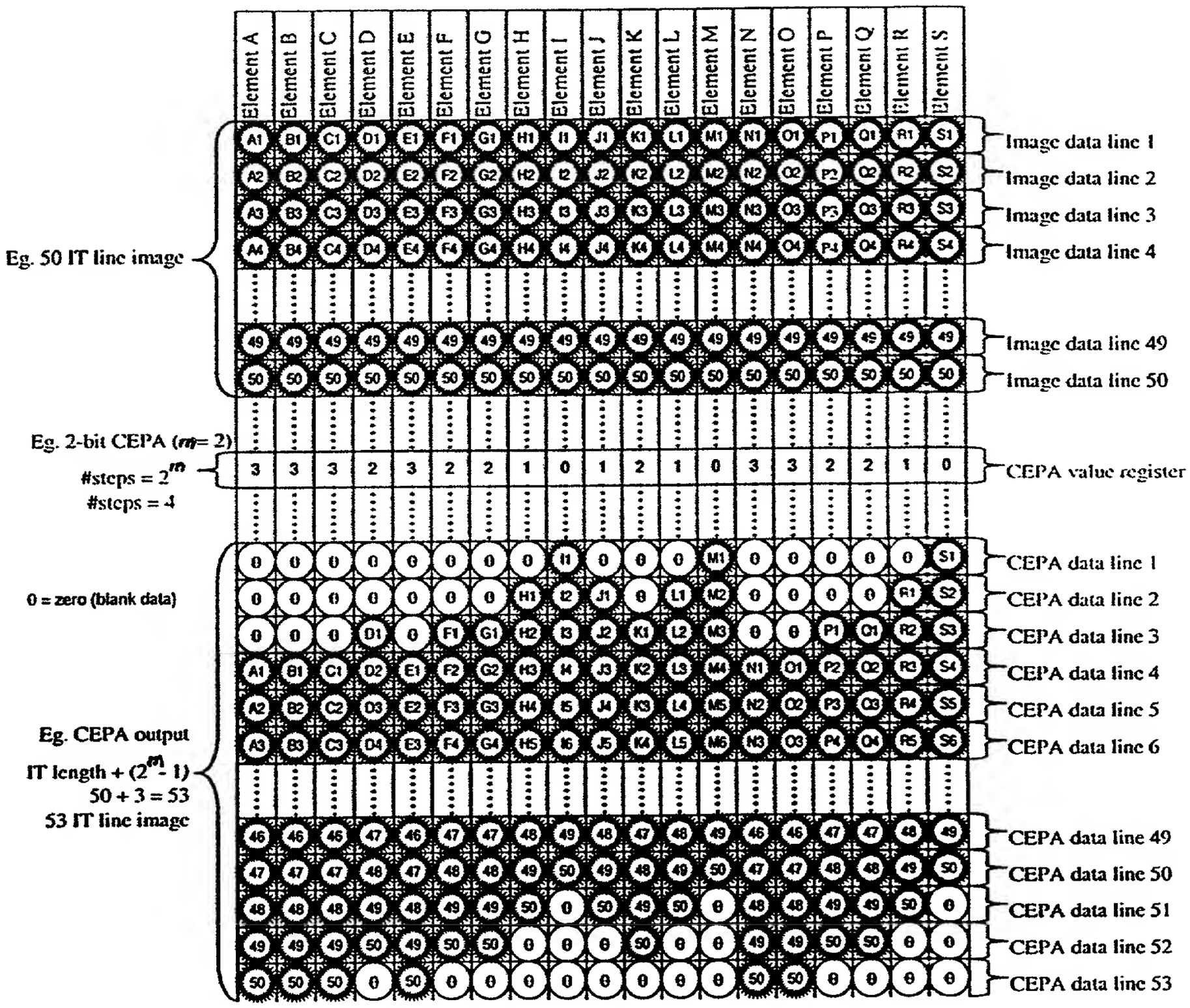


Figure 4 - CEPA data flow diagram

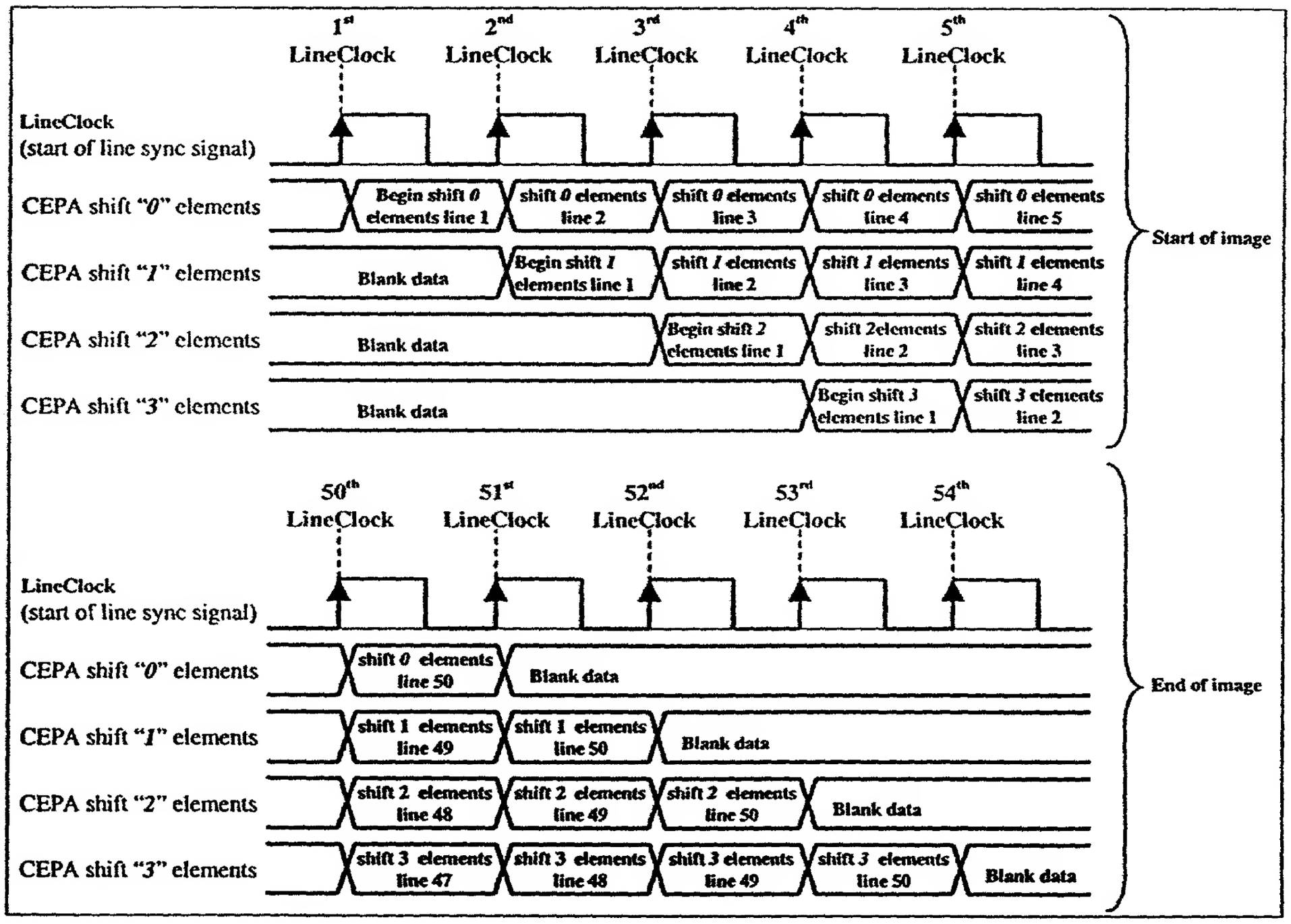


Figure 5 CEPA timing diagram (e.g. 50 IT line image)

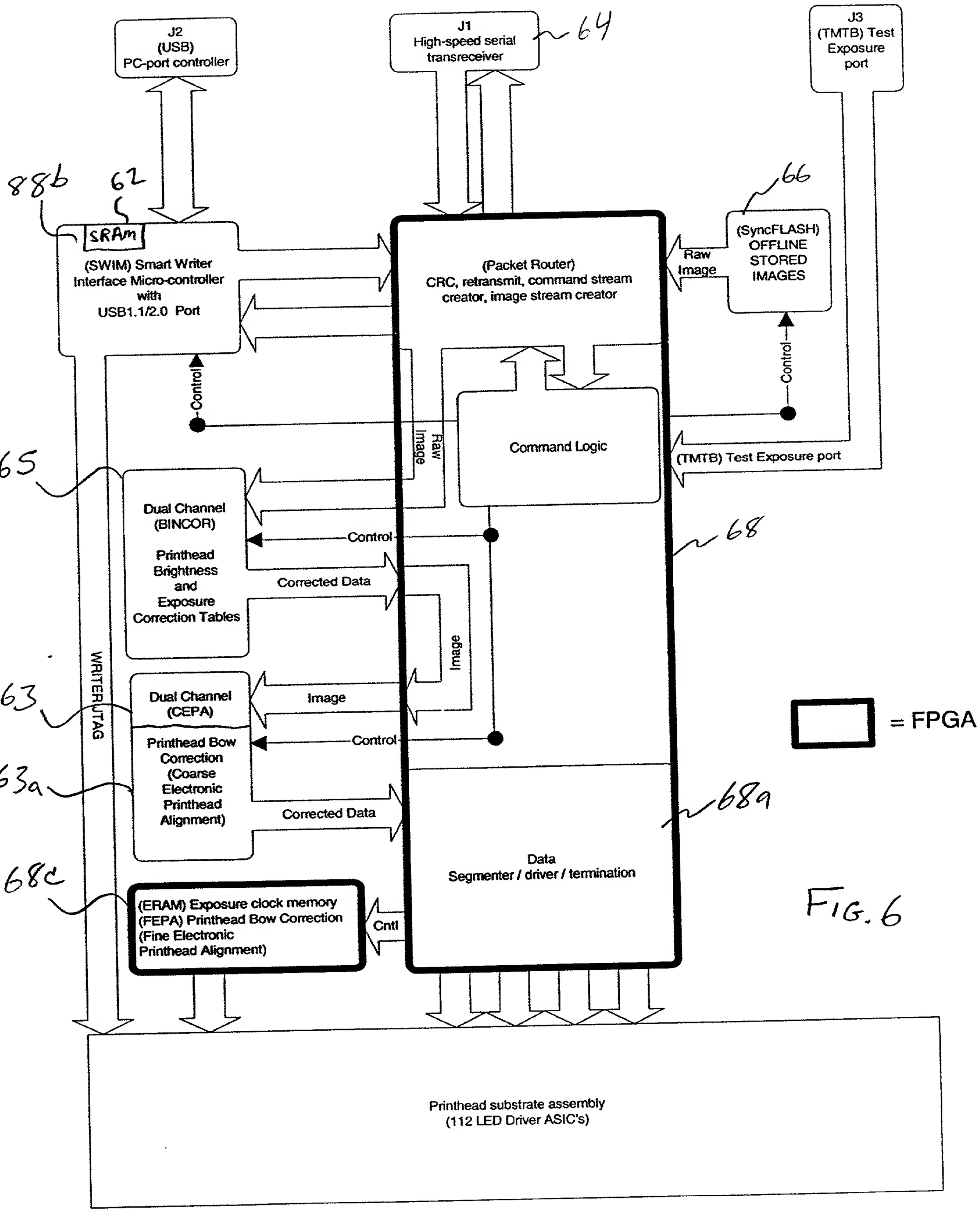

J2
(USB)
PC-port controller
J1
High-speed serial
transreceiver
64
J3
(TMTB) Test
Exposure
port
86b
62
66
SRAm
(SWIM) Smart Writer
Interface Micro-controller
with
USB1.1/2.0 Port
(Packet Router)
CRC, retransmit, command stream
creator, image stream creator
Raw
Image
(SyncFLASH)
OFFLINE
STORED
IMAGES
Control
Control
60
Raw
Image
Command Logic
(TMTB) Test Exposure port
165
Dual Channel
(BINCOR)
Printhead
Brightness
and
Exposure
Correction Tables
Control
Corrected Data
68
Image
WRITER JTAG
163
Dual Channel
(CEPA)
Image
Control
Printhead Bow
Correction
(Coarse
Electronic
Printhead
Alignment)
163a
Corrected Data
68a
Data
Segmenter / driver / termination
68c
(ERAM) Exposure clock memory
(FEPA) Printhead Bow Correction
(Fine Electronic
Printhead Alignment)
Cntl
= FPGA
Printhead substrate assembly
(112 LED Driver ASIC's)

FIG. 6

FIG. 7a

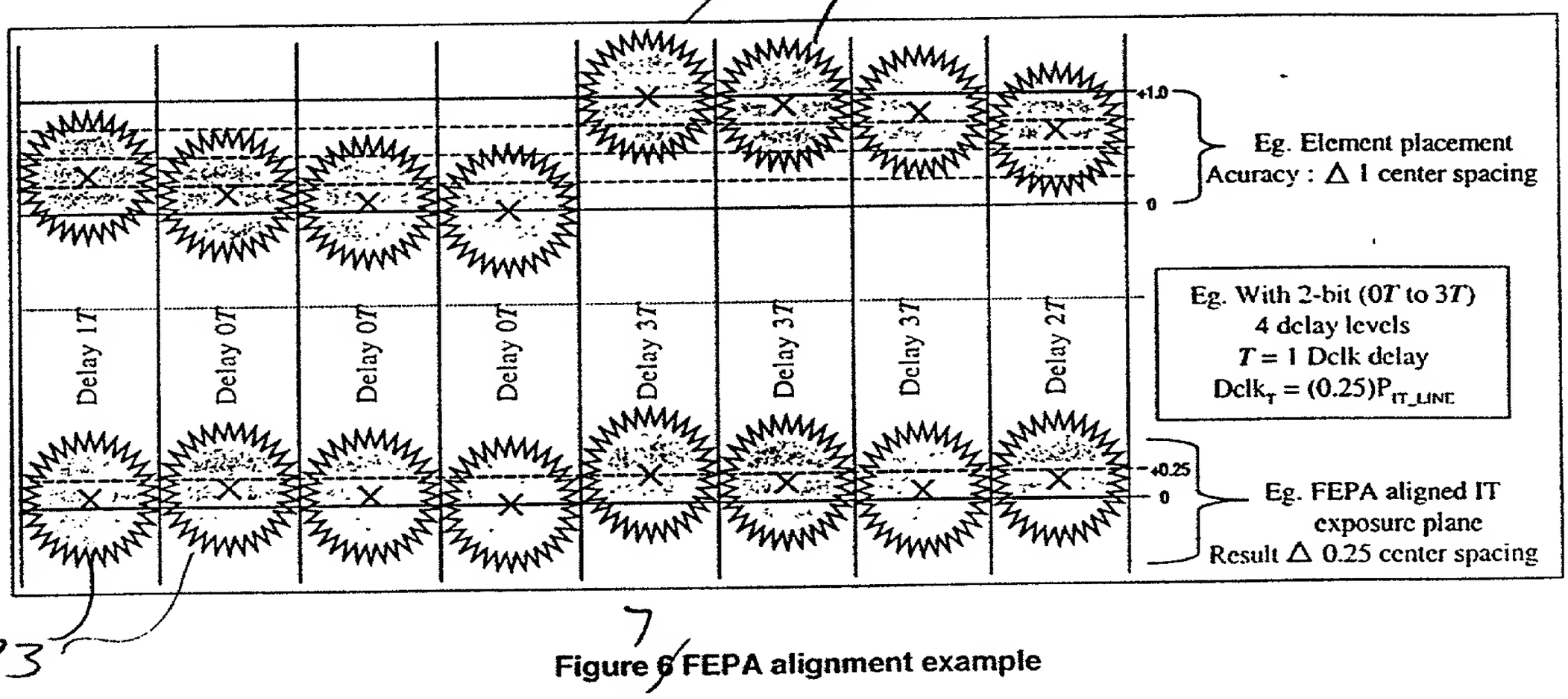


FIG. 7b

Figure 6 FEPA alignment example

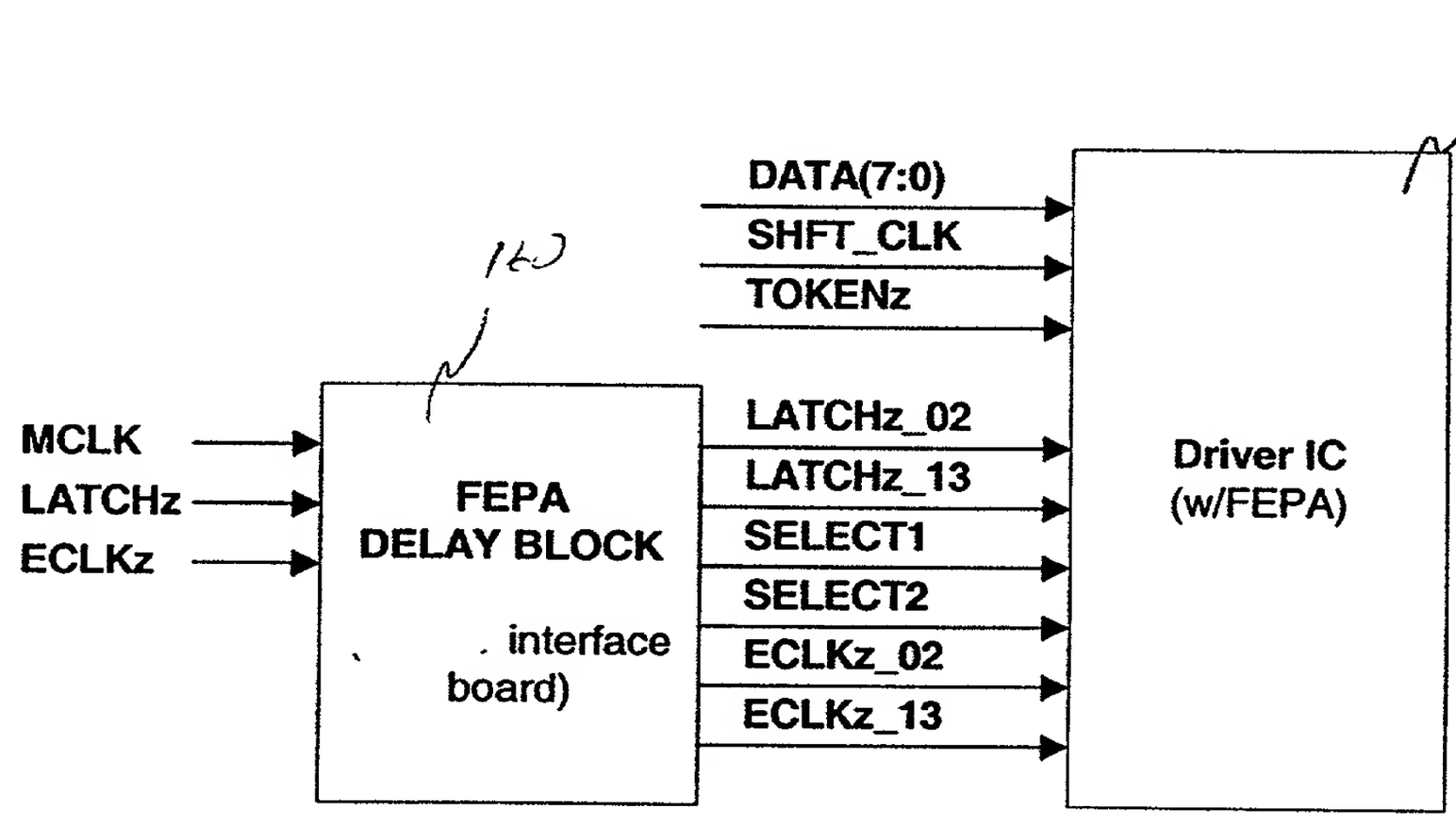


FIG. 8a FEPA BLOCK DIAGRAM

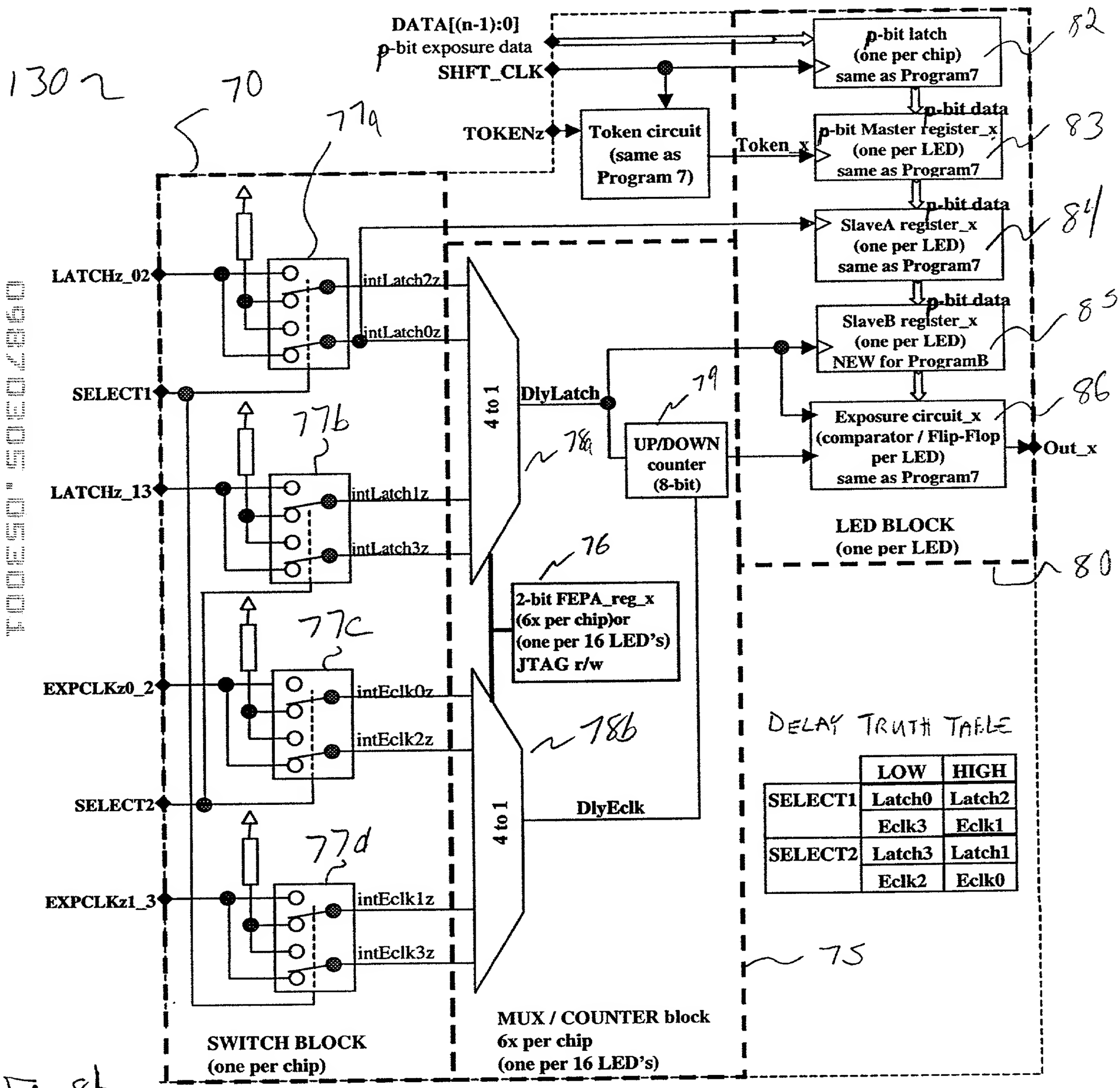

1302
70
77a
DATA[(n-1):0]
p-bit exposure data
SHFT_CLK
TOKENz
Token circuit
(same as
Program 7)
Token_x
p-bit latch
(one per chip)
same as Program7
82
p-bit data
p-bit Master register_x
(one per LED)
same as Program7
83
p-bit data
SlaveA register_x
(one per LED)
same as Program7
84
p-bit data
SlaveB register_x
(one per LED)
NEW for ProgramB
85
Exposure circuit_x
(comparator / Flip-Flop
per LED)
same as Program7
86
Out_x
LATCHz_02
intLatch2z
intLatch0z
SELECT1
77b
LATCHz_13
intLatch1z
intLatch3z
4 to 1
DlyLatch
78a
79
UP/DOWN
counter
(8-bit)
LED BLOCK
(one per LED)
80
76
2-bit FEPA_reg_x
(6x per chip)or
(one per 16 LED's)
JTAG r/w
77c
EXPCLKz0_2
intEclk0z
intEclk2z
78b
SELECT2
77d
EXPCLKz1_3
intEclk1z
intEclk3z
4 to 1
DlyEclk
DELAY TRUTH TABLE
LOW
HIGH
SELECT1
Latch0
Latch2
Eclk3
Eclk1
SELECT2
Latch3
Latch1
Eclk2
Eclk0
75
SWITCH BLOCK
(one per chip)
MUX / COUNTER block
6x per chip
(one per 16 LED's)

Fig 8b

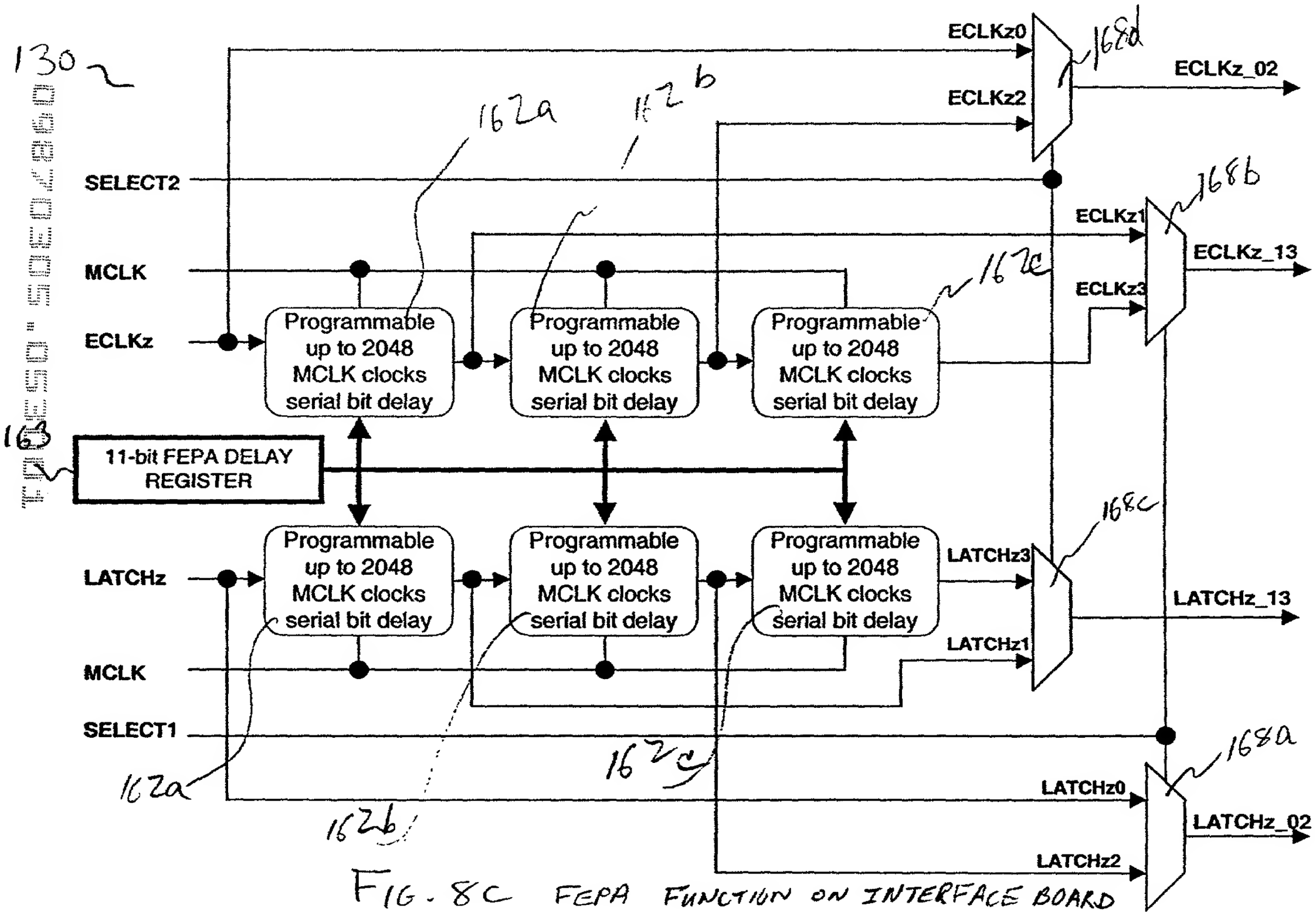


FIG. 8C FEPA FUNCTION ON INTERFACE BOARD

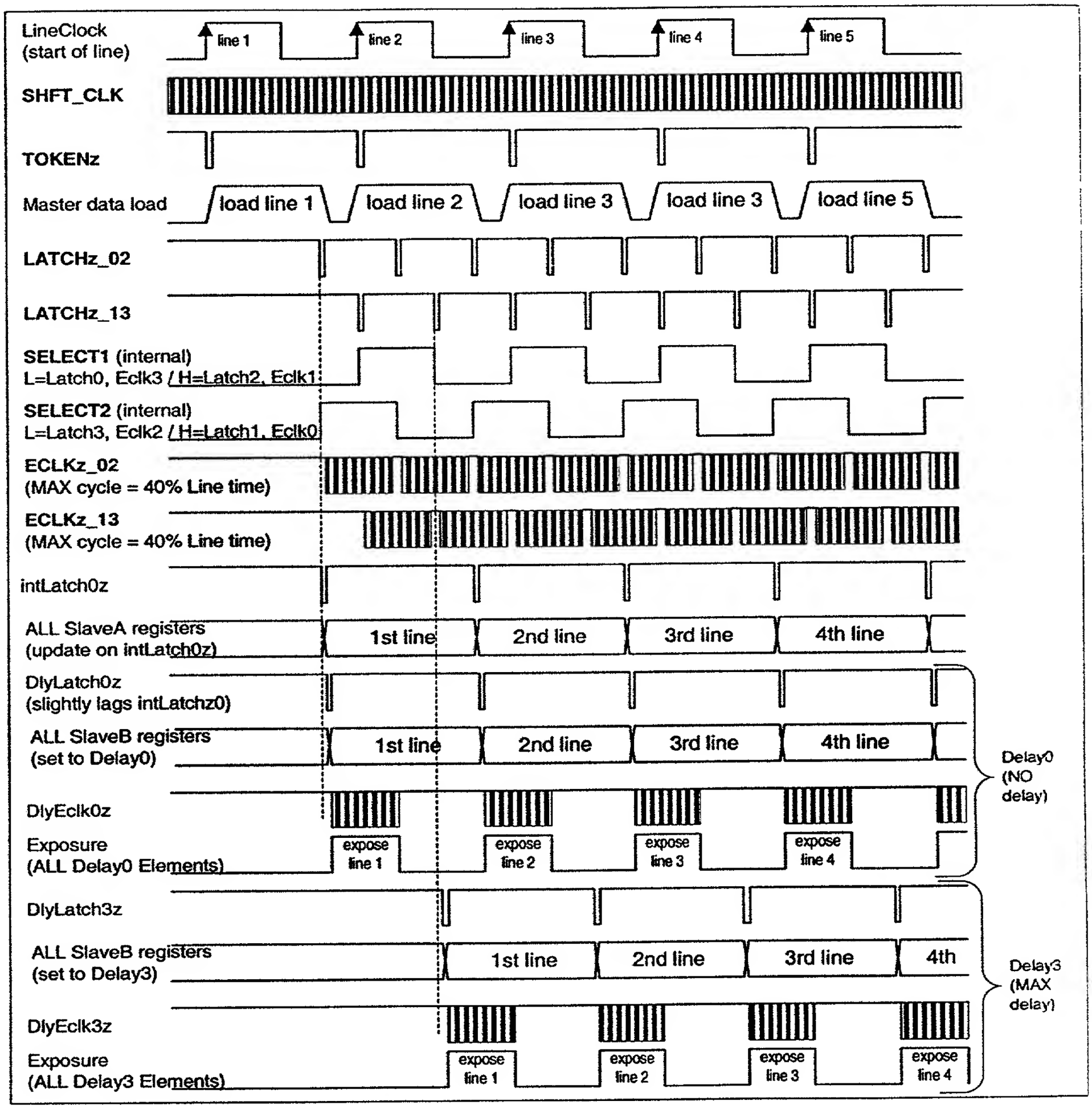

LineClock
(start of line)
line 1
line 2
line 3
line 4
line 5
SHFT_CLK
TOKENz
Master data load
load line 1
load line 2
load line 3
load line 3
load line 5
LATCHz_02
LATCHz_13
SELECT1 (internal)
L=Latch0, Eclk3 / H=Latch2, Eclk1
SELECT2 (internal)
L=Latch3, Eclk2 / H=Latch1, Eclk0
ECLKz_02
(MAX cycle = 40% Line time)
ECLKz_13
(MAX cycle = 40% Line time)
intLatch0z
ALL SlaveA registers
(update on intLatch0z)
1st line
2nd line
3rd line
4th line
DlyLatch0z
(slightly lags intLatchz0)
ALL SlaveB registers
(set to Delay0)
1st line
2nd line
3rd line
4th line
Delay0
(NO
delay)
DlyEclk0z
Exposure
(ALL Delay0 Elements)
expose
line 1
expose
line 2
expose
line 3
expose
line 4
DlyLatch3z
ALL SlaveB registers
(set to Delay3)
1st line
2nd line
3rd line
4th
Delay3
(MAX
delay)
DlyEclk3z
Exposure
(ALL Delay3 Elements)
expose
line 1
expose
line 2
expose
line 3
expose
line 4

Fig 8d

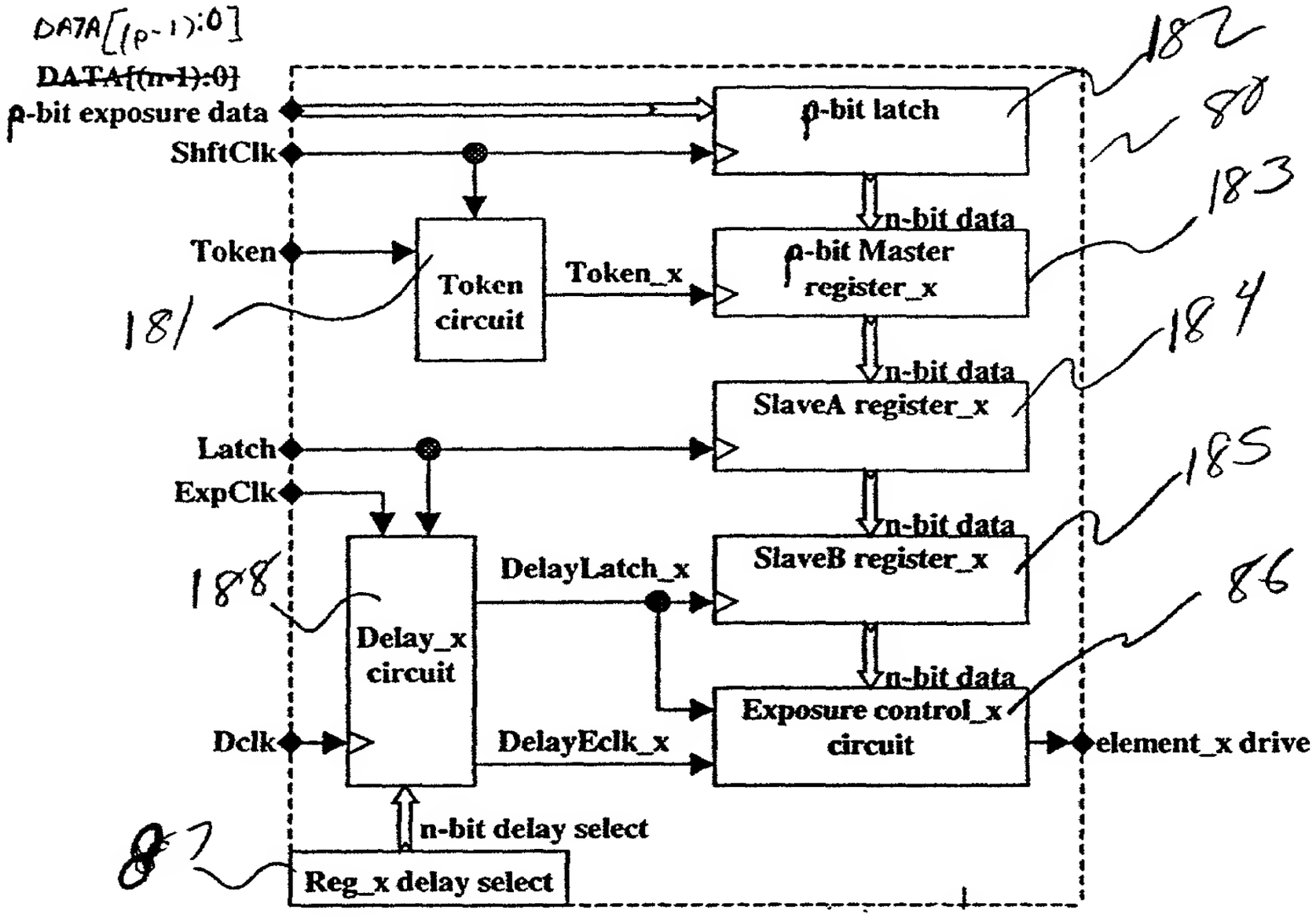


FIG. 9A FEPA DIAGRAM for Second Preferred Embodiment

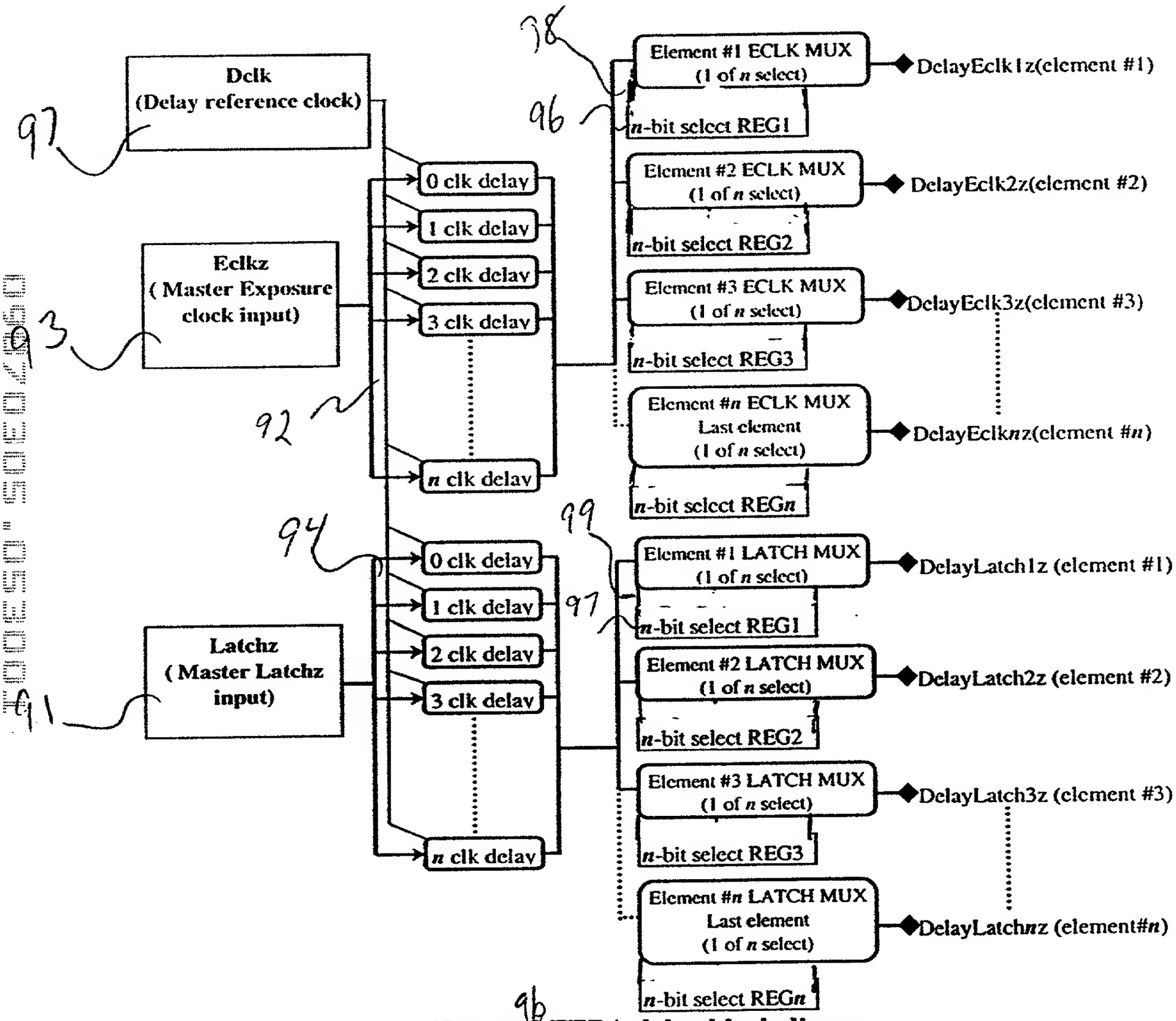
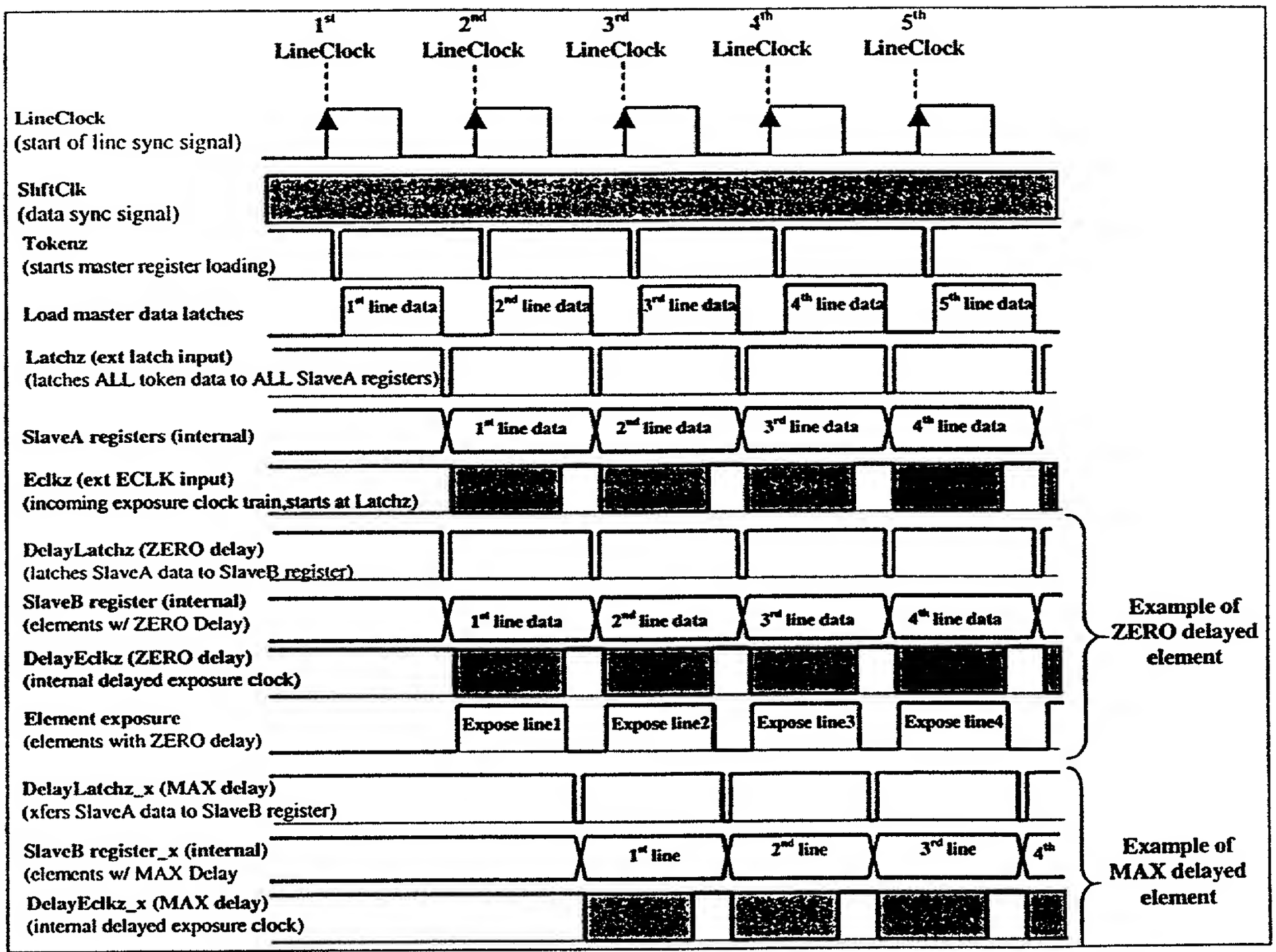
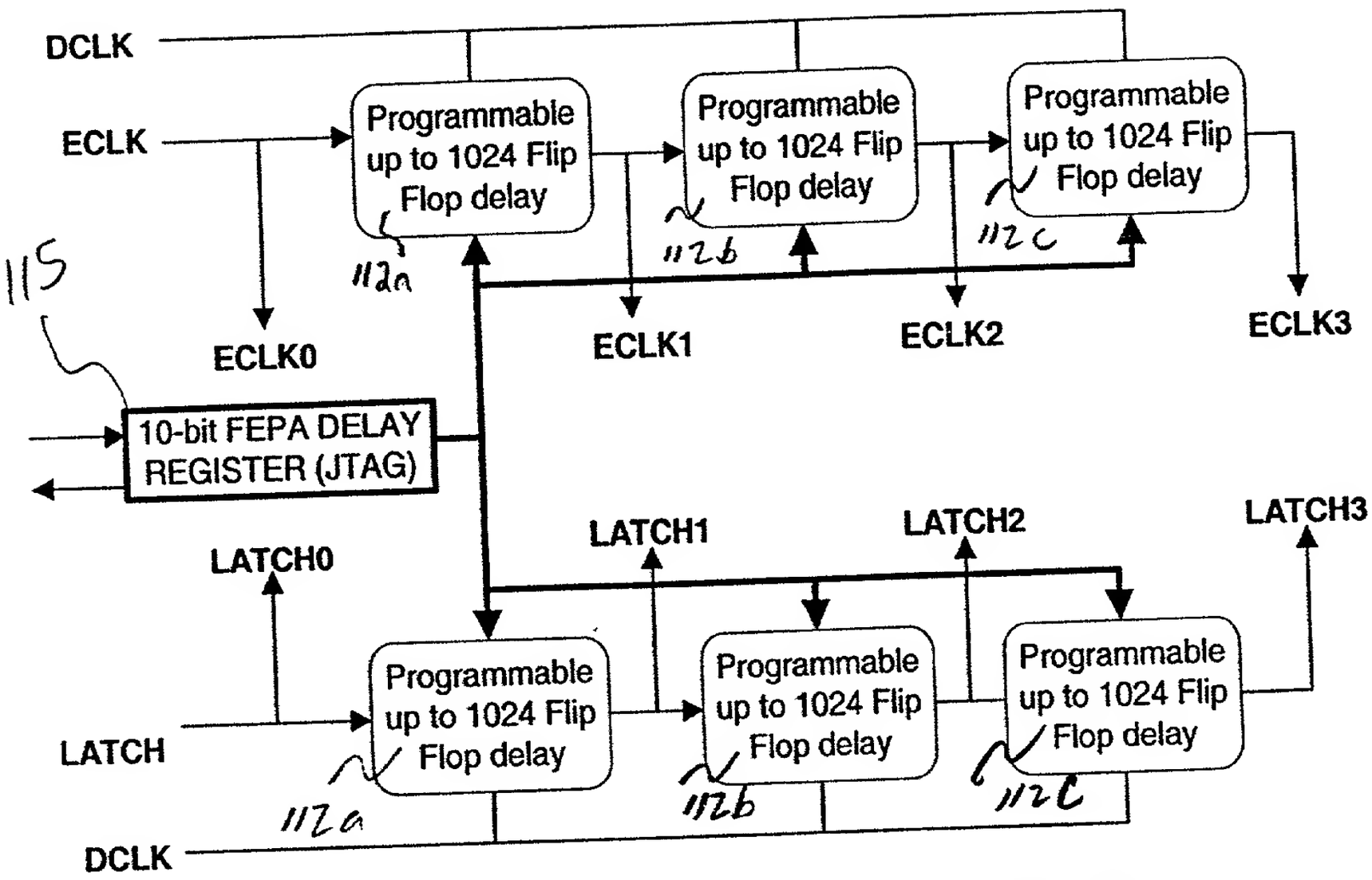


Figure 8 FEPA delay block diagram



10

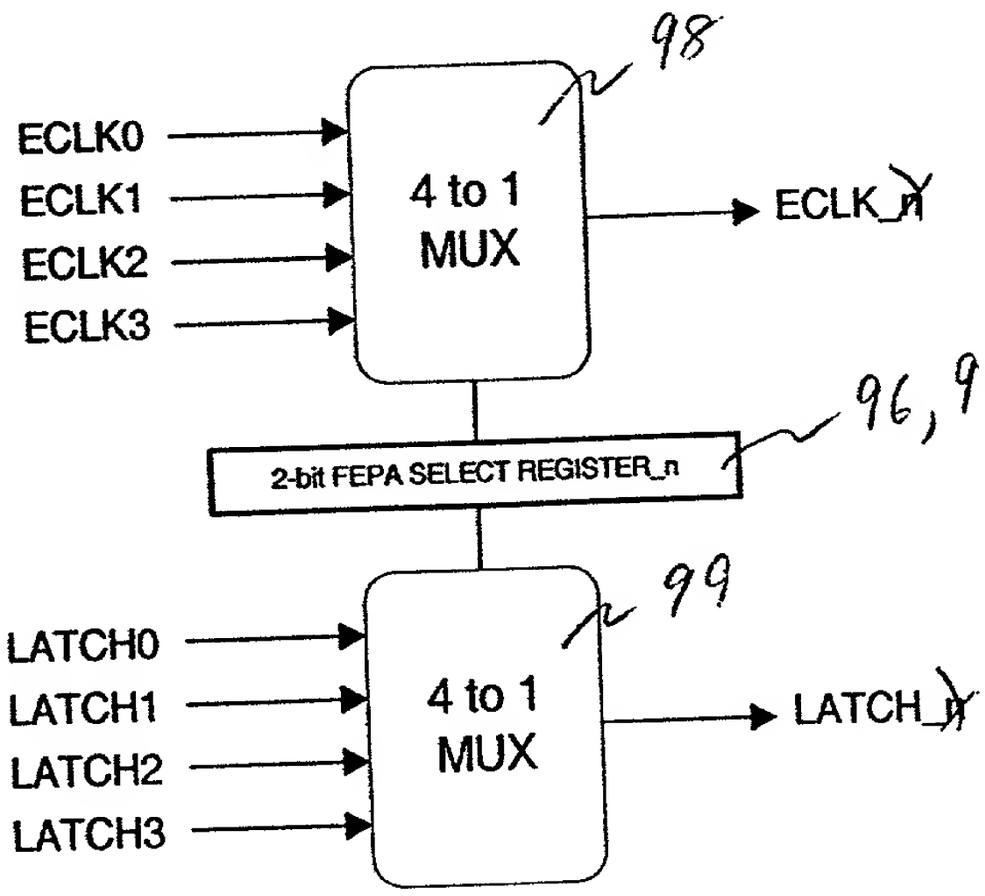
Figure 8 FEPA signal timing diagram



110

FIG. 11

FEPA DELAY CIRCUIT (ONE PER DRIVER IC)

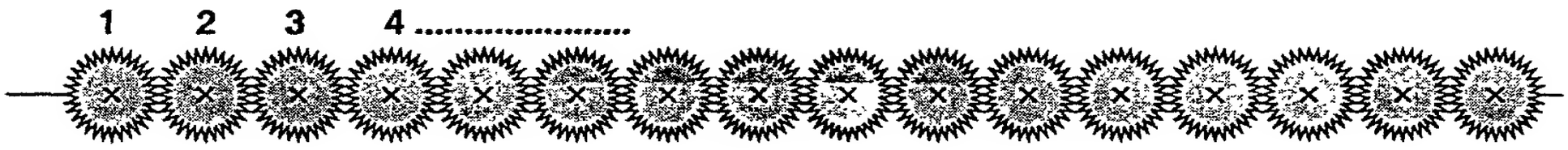


120

FIG. 12

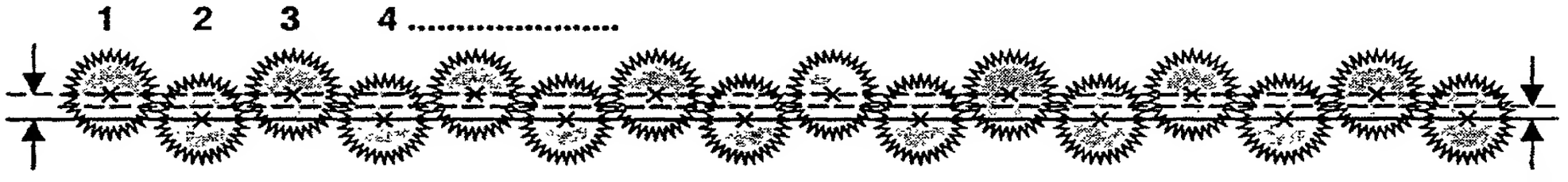
FEPA DELAY SELECT CIRCUIT (ONE PER LED)

FIG 13A



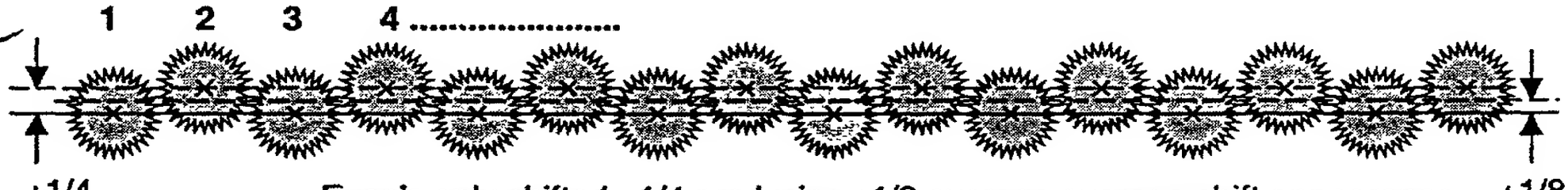
Odd and even shifted same

FIG 13B



Odd's only shifted +1/4 delta producing +1/8 average shift appearance

FIG 13C



Even's only shifted +1/4 producing +1/8 average average shift appearance

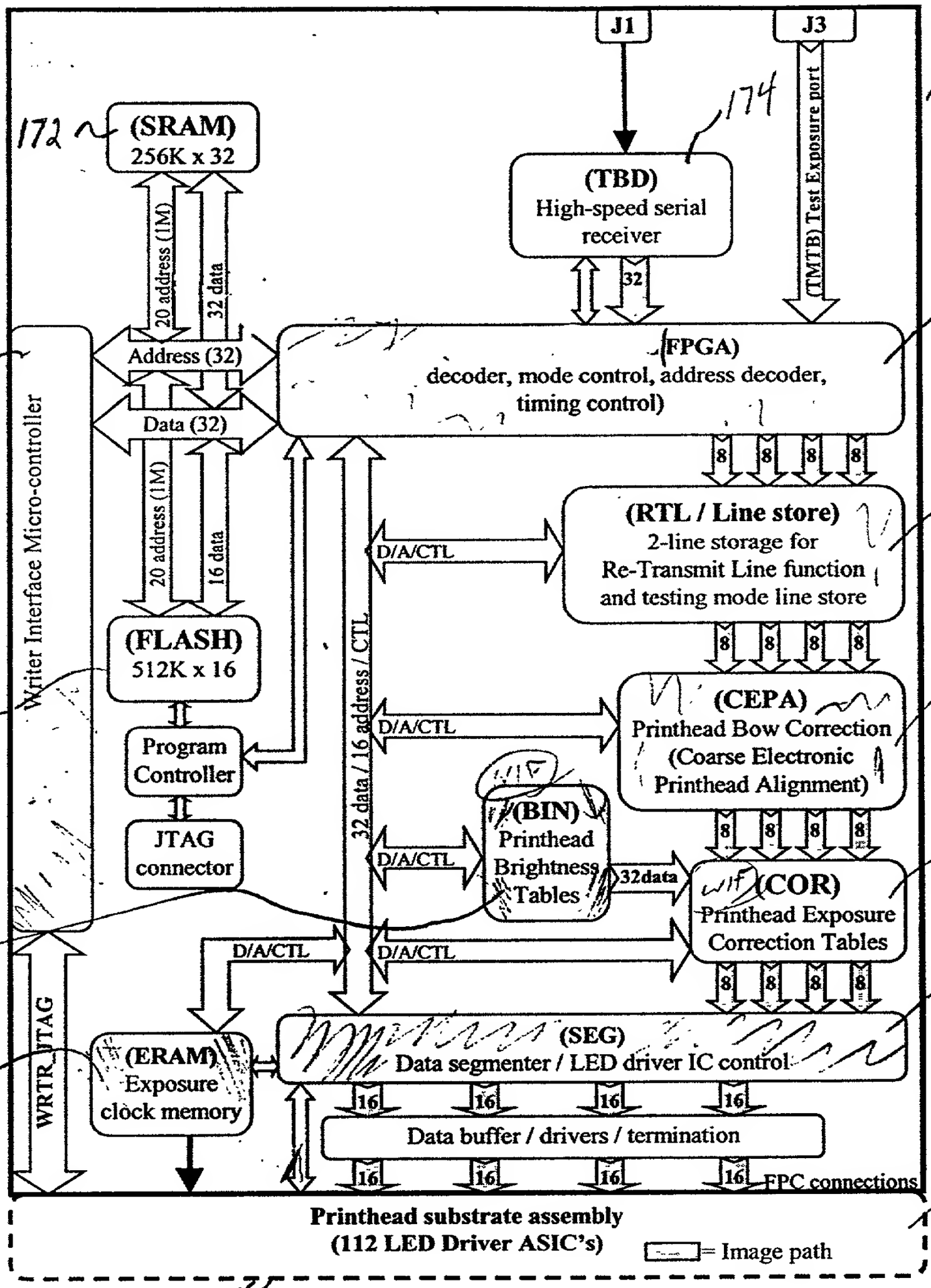


Figure 2A SWIFT board block diagram (FPGA function's shaded)

Interface

FIG. 14